WHAT IS CLAIMED IS:

1. A computer program product for monitoring errors in a system memory of a data processing system, the program product comprising computer executable code stored on a computer readable medium, comprising:

code means for periodically polling a processor of the data processing system to determine if a system memory error has occurred;

code means for retrieving and storing the system memory address associated with the system memory error;

code means for determining a number of consecutive system memory errors associated with the retrieved address and comparing the number of consecutive errors to a predetermined threshold; and

code means for increasing the frequency of polling and increasing the predetermined threshold responsive to the number of consecutive errors equaling the existing predetermined threshold.

2. The computer program product of claim 1, wherein the code means for increasing the frequency of polling and increasing the threshold includes code means for doubling the polling frequency and the threshold each time the number of consecutive errors equals the existing value of the threshold.

3. The computer program product of claim 1, further comprising code means for comparing the number of consecutive errors to a second threshold and, responsive to the number of consecutive errors equaling the second threshold, issuing a system alert.

4. The computer program product of claim 1, further comprising code means for initializing the polling frequency and the consecutive error threshold to initial values prior to initiating the

polling and thereafter resetting polling frequency and the consecutive error threshold periodically, wherein the polling frequency greatly exceeds the resetting frequency.

5. The computer program product of claim 4, wherein said code means for periodically polling comprises code means for implementing a watchdog timer and initiating a polling event at determined intervals of the timer.

6. The computer program product of claim 5, wherein the code means for implementing the watchdog timer comprises code means for initializing a counter and decrementing the counter on every transition of a periodic clock signal.

7. The computer program product of claim 5, wherein the code means for implementing the watchdog timer comprises code means for retrieving real time values from a real time clock and determining a polling interval based on the real time clock values.

8. A data processing system, comprising:

a system memory;

a memory controller coupled to the system memory and a processor coupled to the memory controller, wherein the controller implements error correction circuitry enabled to identify and correct at least some system memory errors;

a dedicated interconnect to provide an interrupt signal to the processor wherein assertion of the interrupt signal interrupts the processor;

a management device coupled to the processor, the management device being enabled to;

periodically assert the dedicated interconnect to interrupt the processor and poll system memory error information, including system memory address information, of the processor following each interrupt;

track the number of errors associated with any particular system memory address;

increase the frequency of said polling if the number of errors associated with a particular memory address equals a first threshold; and

issue a system alert if the number of errors associated with a particular memory address equals a second threshold.

9. The system of claim 8, wherein the management device is further configured to track the number of consecutive errors associated with any particular system memory address and to increase the frequency of said polling if the number of consecutive errors associated with a particular memory address equals a first threshold.

10. The system of claim 8, wherein the dedicated interconnect is connected to a general purpose I/O pin of the management device.

11. The system of claim 8, wherein the management device is configured to double the polling frequency and the first threshold value each time the number of errors associated with a particular memory address equals the existing first threshold value.

12. The system of claim 11, wherein an initial first threshold value is 2 and the second threshold value is 16.

13. The system of claim 12, wherein the period of the initial polling frequency is approximately 600 seconds.

14. The system of claim 11, wherein the management device is further configured to reset the polling frequency and first threshold value to their respective initial values periodically.

15. The system of claim 14, wherein the period associated with resetting the first threshold value is 24 hours.

16. A system management device suitable for use in a data processing system comprising a processor coupled to a system memory, wherein the system management device is configured to

implement a watchdog timer and to assert a signal periodically to interrupt the processor;

retrieve system memory error information including any corresponding system memory address information from the processor following assertion of the signal; and

track the number of system memory errors corresponding to any particular system memory address; and

issue an alert if the number of system memory errors corresponding to a particular system memory address equals a specified maximum value.

17. The management device of claim 16, further configured to assert the signal by asserting a general purpose I/O pin.

18. The management device of claim 16, further configured to track the number of consecutive system memory errors corresponding to any particular system memory address.

19. The management device of claim 16, further configured to increase the frequency of interrupting the processor if the number of errors associated with any particular memory address equals a first threshold.

20. The management device of claim 16, further configured to increase the first threshold value each time the number of errors associated with any particular memory address equals the first threshold.

21. The management device of claim 20, further configured to double the frequency of interrupting the processor and the first threshold value each time the number of errors associated with any particular memory address equals the first threshold value.